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Design and Verification of Advanced Peripheral Bus Protocol Using UVM

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Abstract: The System on chip uses advanced micro controller bus architecture is on chip bus introduced by ARM. Advanced peripheral bus is the component of the AMBA bus architecture. APB is low bandwidth, low power and low performance it used to connect the peripherals like UART, Keypad, Timer and other peripheral devices to the bus architecture. This introduces the AMBA APB bus using UVM architecture design. The design created using the Verilog and HDL and tested by Verilog test bench and design is verified using universal verification methodology. In this, we have a master and a slave. The master sends the control signals as a packet to the slave and the slave addresses the packet if both are equal we are getting transaction of write and read data, Where the master send the address slave recognize and it sends the signal to the master as a read data.

Keywords: APB, AMBA, UVM, HDL, UART

1. INTRODUCTION

The Advanced Microcontroller Bus Architecture (AMBA) is on chip high performance communication bus, it has high power and high bandwidth, and it was introduced by ARM and have two protocols AHB/ASB and APB. The Advanced high-performance bus connected on chip ram and all external devices, which are connected to the bus such as high-performance arm processor, high bandwidth external memory It provides interface to the external bus. System bus provides interface between the AHB put address on bus followed by data it has separate read and write busses. It also supports external off chip and on chip memory. The APB is a low peripheral device, it has low power consumption and lower bandwidth, and supports up to 32 bits and it used in the IoT subsystem, smartphones, networking system on chip, and it supports a wide variety of system on chip with different power, performance and area. To understand how the read and write transfer between the

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master and the slave and designing the protocol with the UVM based and it has more reusability in the test bench in which more number of clients which are not necessary for the designing part in which the UVM can test all the cases and without rearranging the test bench we can change the code here. The objective in the project is to design, implement, and facilitating the development of embedded controller products with one or more CPU to be technology independent and high reusable peripherals. To encourage modular system design to provide the roadmap between peripherals. To minimizing, the silicon infrastructure supports efficiently on-chips and off-chips communication in the operation and the manufacturing. In case of performing complexity programmers, the interface used in the programmer, which develops higher reusability and efficient transfer between the peripherals, here the transfer taking in the bunch of signals [1]

It is an on chip interconnect specification and open standard, which defines the connection and management in functional block of a system on chip It facilitate the development of multiprocessor design with large number of controller and peripherals It uses full duplex parallel communication It having burst transfer High bandwidth control access Higher complexity signal. Whenever slave received the request transaction and not able to complete transaction it indicates master that transaction can be split and save the master number. If the master has more than one pending split transaction it restarts the transaction. In all of these cases, the uvm recognizes the test cases and the environment, performs functionality testing, and then sends the results to the scoreboard, where it checks all of the coverage and number of transactions in the packet, compares them, and if the count, packet, address, and data in both slave and master are equal, the transaction matches and the test cases are passed correctly.

Literature Survey

An on-chip communication protocol includes of a CPU and supporting functions such as oscillators, timers, serial I/O, and analogue I/O, as well as keypad programme memory in the form of NOR flash and usually read/write memory on a single integrated circuit. Computer systems are increasingly being embedded in other machines, such as automobiles, Telephones, and Peripherals for computer Systems, these, are called embedded systems. While, some embedded systems are sophisticated, many have minimal requirements for memory and programing length with no OS, and low software complexity. Rather than having separate connections between each set of devices that need to interact, bus design employs a single data-signaling channel for numerous devices. Rather of having a single set of wires from the CPU for memory and another set for I/O, the data bus is used for data from dynamic ram, into mass storage, and from peripheral devices There is frequently a method for gene device.[4]

The Bus having the control, which could be a quiet, complicate in the numerous asynchronous processes which attempting to share the bus efficiently. Early computer buses were bundle of wires that attached memory and peripheral. They named after electric buses. Usually, there was one bus for memory, and another for peripherals, and these were accessed by separate instructions, with completely different timings and protocols. The Second generation of a bus systems are separated the computer into the two "words", the memory and the CPU on a side, and the various devices on the other side, with in a bus controller in

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between the devices. This is to allow the CPU to increase in speed without affecting the bus; this also moved much more the data out of CPU and into the cards and controller, so device on the bus could talk to each other with no CPU intervention.[2] This is going to lead a much better real-world performance, but also required the cards to be much more complicated. The increasing number of external devices started employing their own bus systems as well. When the Disk is going to drive it was the introduced by the first, and they would add to the machines with the card plugged into the bus, so the computers having many slots on the bus. The bus, known as the "Third Generation," has been on the market since around 2001, including Hyper Transport. They also provide a lot of flexibility in terms of physical connections; thus, they may be used as both internal buses and for linking various equipment. When trying to serve various demands, this might lead to complicated 15 problems because so much of the labour is done by hand.

AMBA Specification

When reading the AMBA specification, pay attention to the following points: Electrical features and technology independence AMBA is an on-chip protocol that is not dependent on the technology used. At the clock cycle

AMBA APB: The AMBA hierarchy of buses includes the APB, which is geared for low power consumption and low interface complexity. The AMBA APB appears as a single AHB or ASB slave device that is encapsulated as a local secondary bus. APB is a low-power system bus extension that directly builds on AHB or ASB signals. The APB Bridge shows up as a slave module that takes care. The APB is set up in such a way that all signal transitions are exclusively connected to the clock's rising edge. This enhancement guarantees that the APB peripherals may be readily incorporated into any design flow, providing the following benefits: It is easy to accomplish high-frequency operation. The clock's mark-space ratio has little effect on performance, and static timing analysis is simplified by using only one clock. Level, the specification solely specifies the bus protocol. Electrical qualities: The AMBA standard contains no information about electrical characteristics because they are very reliant on the manufacturing process technology used for the design. Timing specification: The AMBA protocol specifies the cycle-level behavior of certain signals. The precise timing requirements will be determined by the technology used in the process.

UVM_SEQUENCE: A sequence is created by extending the uvm sequence. It generates a succession of sequence items and sends them to the driver via sequencer.

UVM_SEQUENCER: Between sequences and the driver, the sequencer regulates the flow of request and answer sequence pieces. To communicate transactions, the sequencer and driver use the TLM Interface. The uvm sequencer and uvm driver base classes have seq item export and seq item port declared, respectively. The user must use the TLM connect method to connect them.

UVM_DRIVER: The type of the request sequence item and the type of the response sequence item are both parameterized in the uvm driver class.

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UVM_MONITOR: This monitor is trying to monitor TLM Analysis Port declarations to disseminate captured data to others via a virtual interface handle to the actual interface that this monitor is trying to monitor.

UVM_SCOREBOARD: By comparing the DUT output to the predicted numbers, the scoreboard will determine whether the DUT is valid. The transactions will be received by the scoreboard from the Monitors who have been installed as inside agents. TLM ports and exports will be used to communicate between the monitor and the scoreboard.

Functional coverage: To verify the block and to know the stimulus to utilize is comprehensive enough and that you have covered all of the relevant scenarios/situations to demonstrate that it is working properly? This is where the concept of functional coverage comes into play. System the functional coverage structures in Verilog allow you to measure the completeness of your stimulus by keeping track of the values that have been recorded

Amba Bus Protocol:
The Advanced Micro Controller Bus Architecture bus protocols are a set of interconnect specifications developed by ARM that standardize on-chip communication techniques across various functional blocks (or IP) with the purpose of creating high-performance SOC designs. These designs usually include one or more microcontrollers or microprocessors, as well as a variety of other components, such as internal or external memory. On a single chip, Memory Bridge, DSP, DMA, accelerators, and numerous other peripherals like as USB, UART, PCIE, I2C, and so on are all integrated. The main goal of AMBA protocols is to create a common and efficient approach to connect these blocks that can be reused across many designs. Understanding where these distinct protocols are utilized, how they originated, and how they all fit into a SOC design is the first step in studying AMBA protocols. A conventional AMBA-based SOC design using the AHB (Advanced High Performance) or ASB (Advanced System Bus) protocols for high bandwidth connectivity and an APB (Advanced Power Bus) for low bandwidth interconnect is shown in the diagram below (reference from the AMBA 2.0 document). With the rising number of functional blocks integrating into SOC designs, shared bus protocols began to reach their limits sooner, and in 2003, AMBA 3 was updated to include a point-to-point connectivity protocol — AXI (Advanced Extensible Interface). In 2010, AXI 4 was released, which was an improved version. This evolution of protocols is depicted in the diagram below.

On a shared bus, the Advance High-performance Bus is used to connect components that require more bandwidth. Internal or external memory interfaces the direct memory and so on could be used, but the common bus would limit the number of agent. This is a shared bus protocol for numerous masters and slaves, similar to APB, however burst data transfers allow for larger bandwidth.
The AMBA bus AHB is a new generation of AMBA bus that is designed to meet the needs of there are no burst data transfers available. The most recent specification (APB 2.0) is available on the ARM website here. The AMBA APB appears as a single AHB or ASB slave device that is encapsulated as a local secondary bus. APB is a low-power system bus extension that directly builds on AHB or ASB signals. The APB Bridge appears as a slave

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module that manages the local peripheral bus's handshake and control signal retiming. By starting from the beginning, the APB interface may be defined. Many ASIC libraries offer a wider range of rising edge registers. The APB has been updated to make it easier to interact with the new AHB. A single APBbridge is generally included in an AMBA APB implementation to convert AHB or ASB transfers into a format appropriate for the slave devices on the APB.

Difference between AHB and APB:

	AMBA AHB	AMBA APB
Feature	•High performance •Pipelined operation •Multiple bus masters •Burst transfers •Split transactions •Single cycle bus master handover •Single clock edge operation (rising edge) •Wider data bus configuration	•Low power •Latched address and control •Simple interface •Suitable for many peripherals •Single clock edge operation (rising edge)
components	•AHB master •AHB slave •AHB arbiter •AHB decoder	•APB bridge (slave on AHB or ASB) •APB slave

AMBA APB Signal

Signal	Source	Description
PCLK	Clock source	the rising edge of the PCLK times- All transfers on the APB
PRESETN	System bus	The APB reset signal is active Low
PADDR	APB Bridge	This is the APB address bus. It can be Up to 32bitwide
PSELX	APB Bridge	The APB master select the peripheral Devices
PENABLE	APB Bridge	This indicates the transfer between the devices
PWRITE	APB Bridge	APB write access when high and an APB read access when low.
PWDATA	APB Bridge	32-bit write data. During write cycles when PWRITE is high.
PRDATA	Slave interface	32-bit read data. It gives the signal

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		to the master
PREADY	Slave interface	when ready is high then slave Becomes active write/read

Operating State: APB Bridge

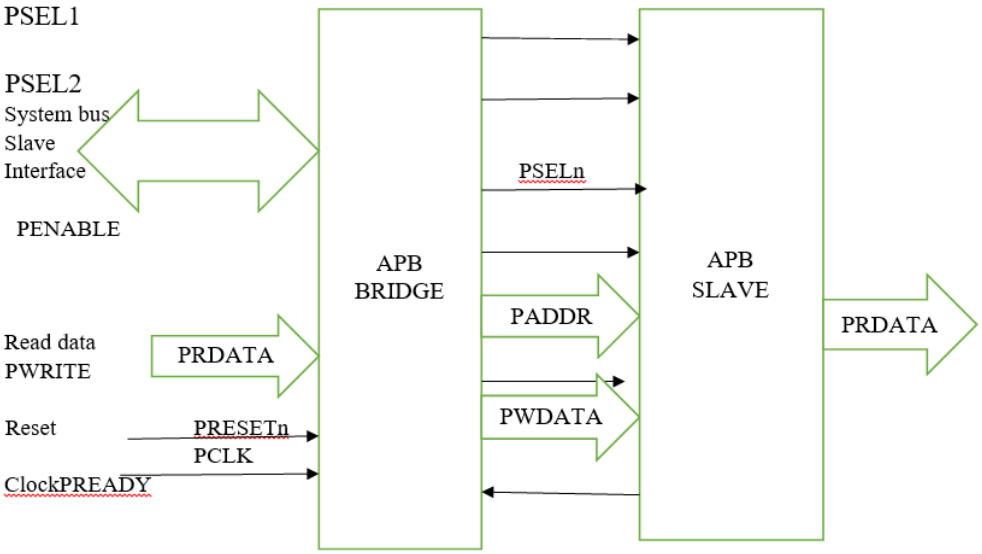

Fig 1: APB Master

1) The addresses that are locked and held until all transfers are completed
2) It modifies the address signals and creates the PSELx peripheral select signal, which drives data to the APB for a write transfer

APB Slave

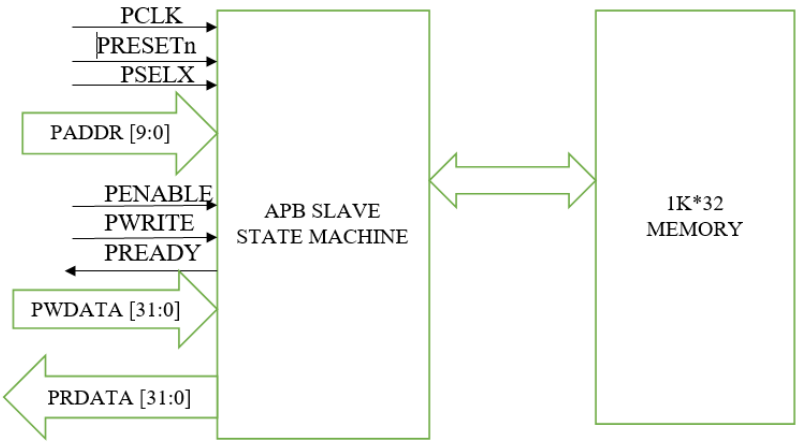

Fig 2: APB Slave

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State Machine

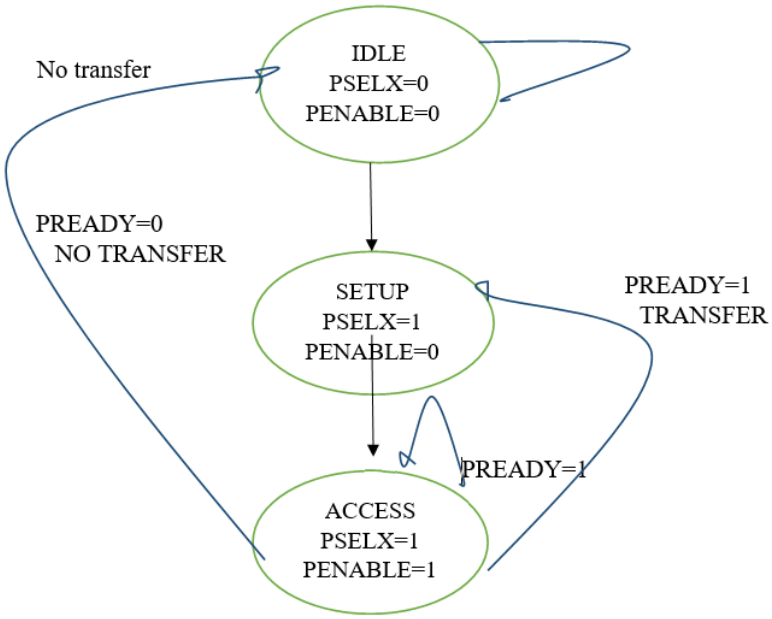

Fig 3: APB State Machine

APB Write Access

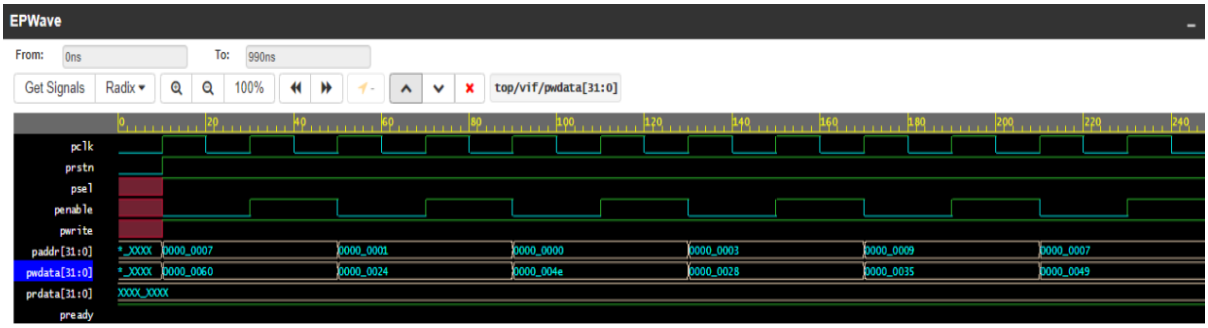

Fig 4: APB Write Transfer

The figure indicates that during the first clock cycle, it is in the idle state and during the second clock cycle, it is in the setup phase, when the master selects the peripherals, so select is set to high, and we are supplying address and data, but enable is set to low. The enable is high throughout the other clock cycle, and the transaction is completed, but the ready signal is not so in the next cycle, the ready is high and the data is written in the slave

APB Write Access with Wait:

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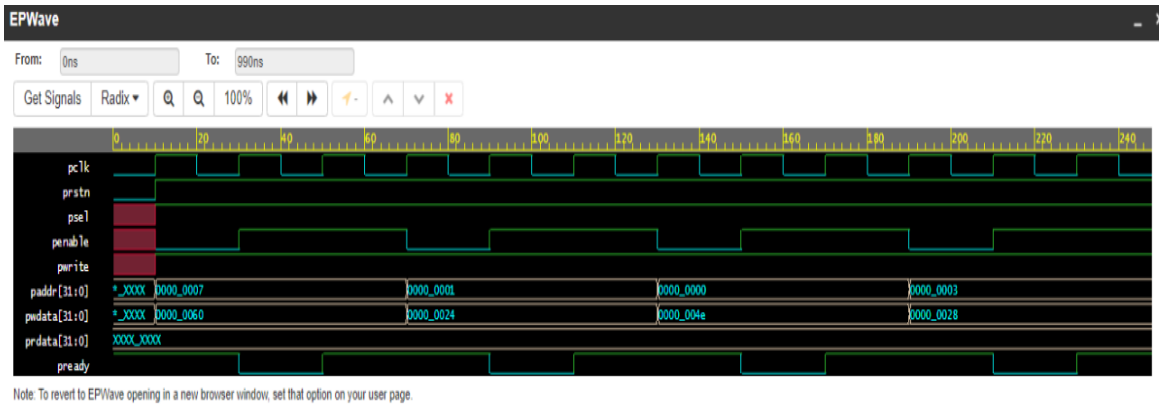

Fig 5: APB Write Transfer with Wait States

APB Read Access

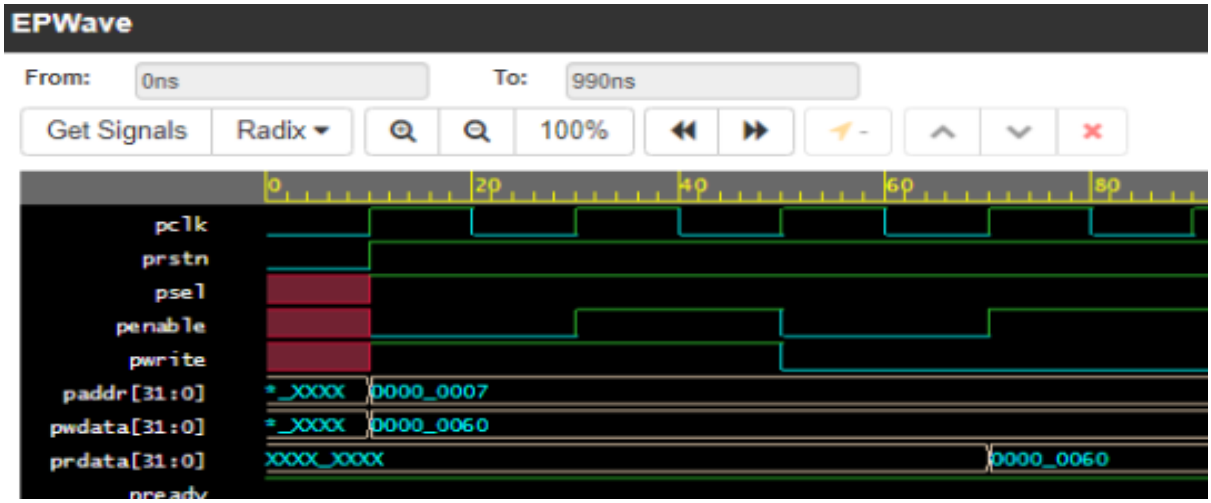

Fig 6: APB Read Transfer

APB Read Access with Wait:

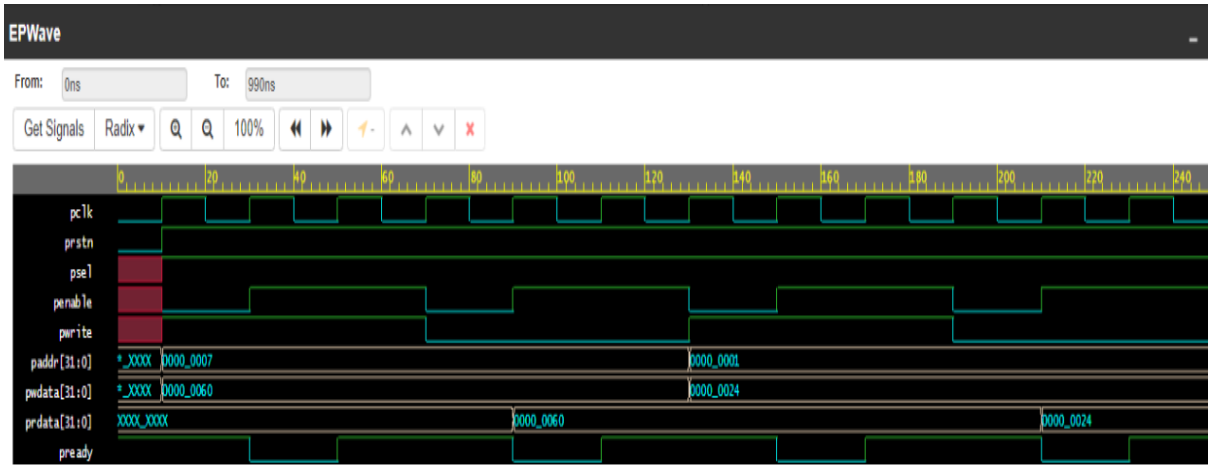

Fig 7: APB Read Transfer with Wait States

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The figure 6 and 7 indicates that during the first clock cycle, it is in the idle state and during the second clock cycle, it is in the setup phase, when the master selects the peripherals, so select is set to high, and we are supplying address and data, but enable is set to low. The enable is high throughout the other clock cycle, and the transaction is completed, but the ready signal is not so in the next cycle, the ready is high then slave will give the read signal to master and write should low.
Results:

2. CONCLUSION

The entire project deals with the design of advanced peripheral bus protocol using uvm using the test bench environment. The APB is designed using the Verilog HDL is built by the integrating all the verification components and communicating with each ports. It verified the read and write in the proper flag triggers and comparing with DUT output and the reference model output weather us getting the correct functionality.

Advantages: Low complexity signals Low power consumption Simple for interface

Disadvantages: APB doesn't support Multiple transfers. APB does not support for burst transfer and low throughput.

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