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Low Power D Flip Flop Design for VLSI Applications

A. Manikandan*

**Assistant Professor, ECE Department, SSM Institute of Engineering and Technology, Dindigul, India*

*Corresponding Email: *manikandan.aapece@ssmiet.ac.in*

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Abstract: ***A flip-flop is a basic storage element used to store information. It is used to build RAM, latches, shift registers, counters, and other digital circuits. This paper proposes a new innovative design for D flip-flops. This design consumes much less power than previous flip-flop designs. The first proposed design introduces two gate-leakage transistors at the output gate using the GALEOR method. The second proposed design uses ONOFIC technology. Therefore, compared to the previous design, the power consumption of Design-I and Design-II is reduced by 35.61% and 34.36%, respectively. The proposed design is simulated using a Cadence tool using 90nm CMOS technology operating at 500MHz.***

Keywords: Flip-Flop (FF), DTCMOS, LECTOR, GALEOR, ONOFIC.

1. INTRODUCTION

With the development of mobile applications and battery-operated devices, reducing the power consumption of these devices is a fundamental issue [1-4]. Therefore, the power consumption of VLSI circuits must be reduced to improve the performance of these devices. To reduce power consumption, many researchers devised different methods at different stages of the VLSI design cycle. Flip-flops are the basic storage elements used in digital systems [5-8]. Flip-flops in digital systems consume about 20-45% of the total system power. Therefore, the design of flip-flops is of great significance for improving the power consumption performance of digital systems [9]. Various flip-flop designs have been developed over the years. Flip-flops using transmission gates are the most commonly used flip-flops [10]. True single-phase clock (TSPC) flip-flops have emerged to overcome the high clock loading problem in this design. Flip flops are fundamental memory elements employed in digital systems [11].
The power consumed by flip flops in digital systems is around 20-45% of total system power [12]. Thus flip flop designs are crucial in enhancing the power consumption performance of the digital systems. Various flip flop designs have been developed over the years [13]. The

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flip flop using transmission gate is the most commonly used flip flop. To overcome the high clock loading problem that exists in this design, true single- phase clocking (TSPC) flip flops came into picture [14]. A number of low power techniques have been worked upon by researchers such as dual threshold CMOS (DTCMOS) technique, multithreshold CMOS (MTCMOS) technique, transistor stacking, LECTOR etc [15]. This paper proposes new designs for D flip flop using GALEOR and ONOFIC approach. The proposed designs are enhancement of the LRFF (Logic structure reduction Flip Flop) design and use single phase clock for operation. This paper has been divided into five sections. Section II has a review of previously designed typical master-slave flip flops. The proposed flip flop design has been discussed in section III. In section IV performance indices and simulation results have been tabulated. Section V concludes the paper.

Literature Review

Researchers have studied many galvanic technologies such as DTCMOS (dual threshold CMOS) technology, MTCMOS (multiple threshold CMOS) technology, transistor stacking, LECTOR. The proposed design is a modification of the LRFF (Logical Structure Reduced Flip-Flop) design and operates using a single-phase clock [16]. This document is divided into five parts. The second part considers a previously designed general-purpose master-slave flip-flop [17].

Many flipflop designs are reviewed, where Fig.1 shows a conventional master slave type flip flop using transmission gate In this design there is drawback of high capacitive clock loading. Due to which there is a higher power consumption even in case of low data activity or static inputs [18]. In Fig.2 shows the circuit of a flip flop based on Adaptive Coupling scheme (ACFF).Here a differential latch structure has been used along with pass transistor logic. Instead of transmission gates nor p-type pass transistors are used [19].

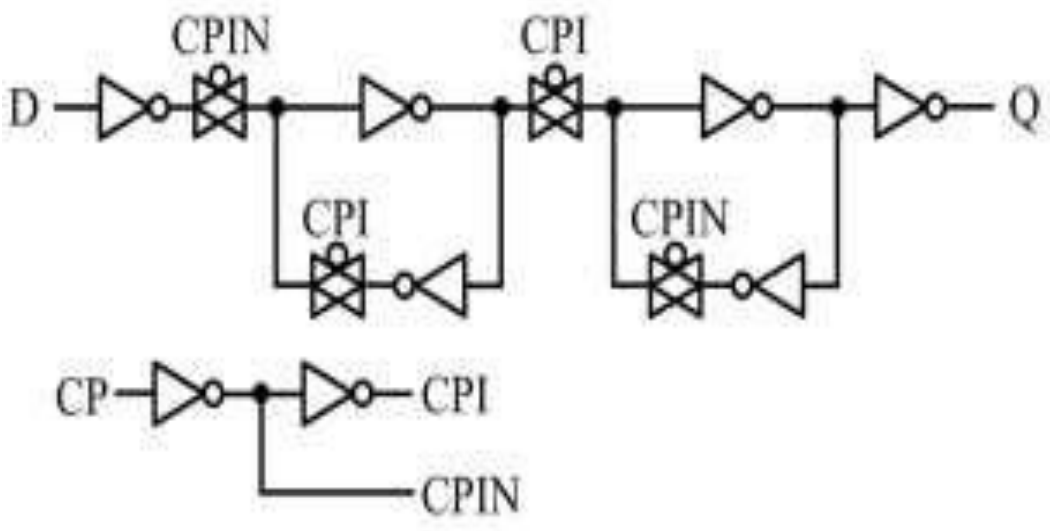


Fig.1. Transmission-gate flip flop

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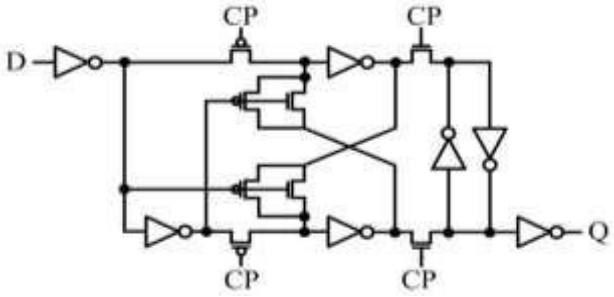


Fig.2. Adaptive Coupling flipflop (ACFF)

A total of 22 transistors are used and the clock drives only four transistors. The pair of circuit for level restoration at master latch as a longer setup time. Also, there is a problem of power leakage ascertain input combinations [20].

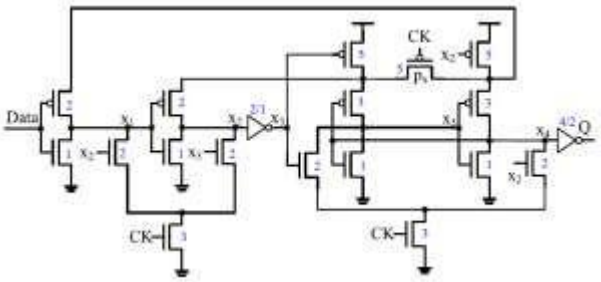


Figure 3 Phase Compression Flip-Flop (TCFF)

Another flip flop design employing topologically compressed technique (TCFF) is shown in Fig.3.The design is obtained by simplifying combinational type circuit on the basis of logical equivalence.
The circuit uses single phase clock. The transistor count is 21 and the clock drives only three transistors. The design has a longer setup time as only two p-MOS transistors constitute a weak pullup network [21].

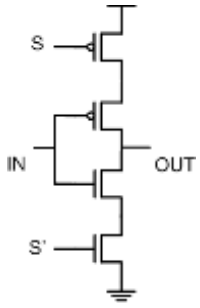


Fig.4 Logic structure Reduction flipflop (LRFF)

The logic structure of the reduced flip-flop (LRFF) showed in Figure 4 uses CMOS logic and complementary pass-transistor logic. An extra discharge path is provided between them as latch and the slave latch which enhance the timing parameters. Also there were no floating

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internal nodes while the circuit was in operating state which reduced the leakage power consumption. The circuit suffered from poor hold time performance [22].

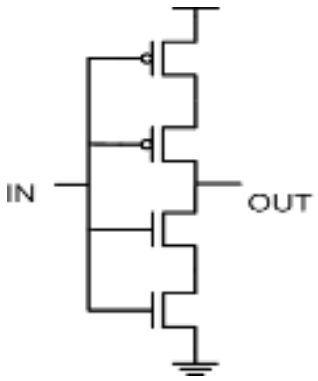


Fig.5 Sleep transistor technique applied to inverter

To solve leakage power problem researchers have come up with various schemes. In Dual threshold CMOS (DTCMOS) technique devices that have low threshold voltages are used on paths with high delay while for other paths, transistors with high threshold voltages are utilized [23]. In Multithreshold CMOS (MTCMOS) high threshold devices are inserted between supply voltage and ground. These devices are switched off during standby mode which shuts down the powers supply to the circuit. This method is commonly known as Sleep Transistor. The need for complex control circuitry limits the use of sliding transistors [24].

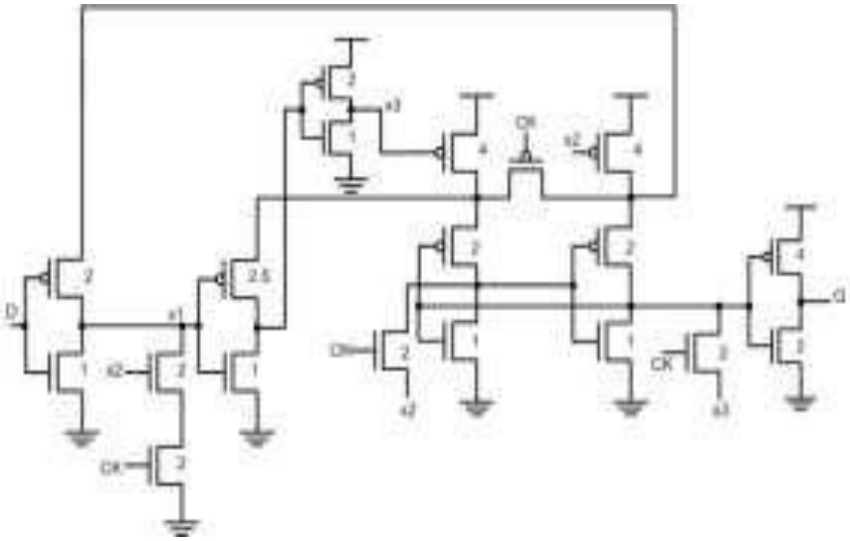


Fig.6 Forced stack technique applied to inverter.

Another way to lower down the leakage current is the use of transistor stacks. In forced stacking, a transistor is replaced by two transistors whose width is half of the previous transistor. Thus when two or more transistors in series are turned off at the same time, leakage power is reduced. However, in this the propagation delay increases [25].

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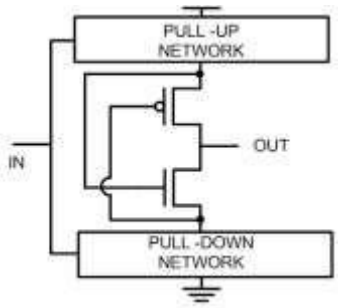


Fig.7 LECTOR method

LECTOR technology inserts two transistors between the pull-up and pull-down circuits that control leakage current [26]. The two transistors are arranged in such a way that one of them is always off. Thus, there is an increase in off transistor count creating stack effect. Anyhow, sizing the sleep transistor correctly is important. GALEOR technology inserts p-MOS and n-MOS transistors in the pull-up and pull-down circuits. In both transistors, the gate is controlled by the drain. GALEOR technique introduces stacking effect and there by reduces leakage power [27].

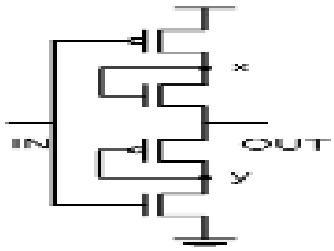


Fig.8 GALEOR technique

In ONOFIC (On/Off logic) approach there is an insertion of On/Off logic circuitry consisting of an n-MOS and p-MOS transistor. The ONOFIC circuit provides a good conduction path when turned on and a good resistance when turned off. This reduces leakage power when inactive and when the circuit is operating in standby mode [28].

Proposed Work

The proposed D flip-flop design is an improvement over the LRFF (Logic Structure Reduced Flip-Flop) design with significantly improved power consumption. The GALEOR technique is used in Design-I to reduce leakage power loss through the inverter (the output gate of the flip-flop). In the proposed design, two transistors are introduced between the n-MOS and p-MOS of the output inverter, as shown in Figure 10. When IN=0, the n-MOS is in off condition. Thus at node y the voltage becomes close to Vdd. This in turn switches off the gated leakage p-MOS transistor. As a result a two transistor stack is formed which decreases the flow of leakage current. Similarly when IN=1, the p-MOS transistor is turned off. A voltage close to 0, formed at node lower the power dissipation.

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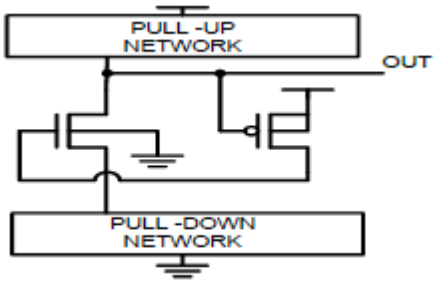


Fig.9 ONOFIC technique

Design-II

In the second proposed design, On/Off logic (ONOFIC) technique has been employed. It uses single threshold voltage transistors. An additional logic is added in the output inverter, which is controlled by the input combinations. The ONOFIC logic circuit has an n-MOS and a p-MOS transistor connected in a way shown in Fig.10. In the ONOFIC logic block, the connections are made such that when the inverter input is logic low, both the n-MOS and p-MOS transistors of
ONOFIC logic are turned off. This increases the resistance of the path from VDD to ground. When the inverter input is logic high, both the n-MOS and p-MOS transistors of ONOFIC logic are turned on and a logic low is achieved at the output. Thus, there is a decline in power dissipated by the circuit without any degradation in the output logic levels.

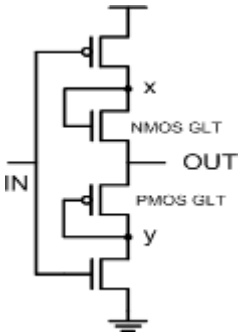


Fig.10 Arrangement of gated leakage transistors (GLT)

2. EXPERIMENTAL RESULTS

The proposed D flip-flop design was implemented using 90nm MOSFET technology and evaluated using Cadence Virtuoso tools. Simulated power level at 500MHz frequency at 27°C. The power loss of the proposed Design-I at 100% switching activity is 35.61% lower than that of the L RFF design. In transient response, the output waveform has a reduced voltage wing. Compared to Design I, the second proposed design addresses the reduced output voltage swing at the cost of almost no power increase. Compared with LRFF, the power loss of the proposed Design II is reduced by 34.36%. Table 3 shows the average power loss, delay, and comparison between the PDP-based LRFF design and the proposed design a shown in Figures 11 and 12.

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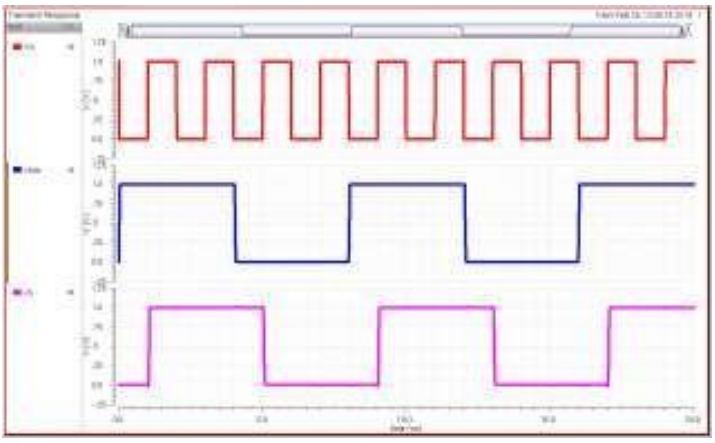
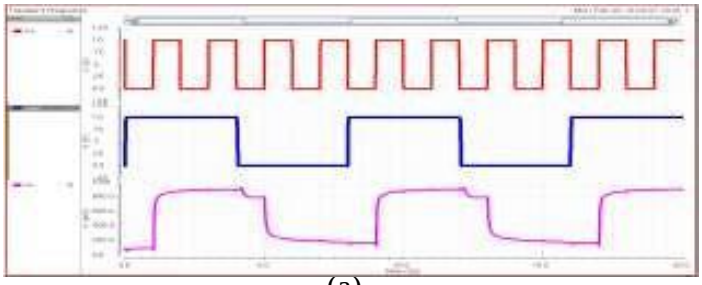
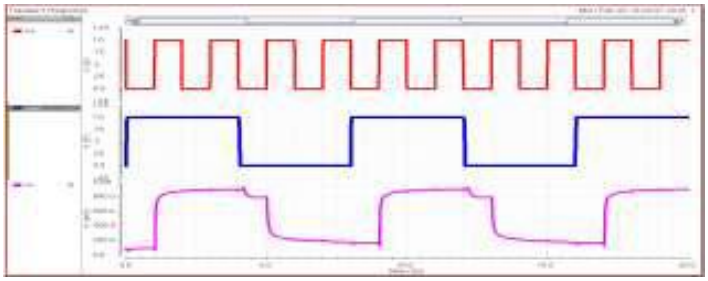


Fig.11 Simulation wave forms of LRFF



(a)



(b)

Fig12.Simulation wave forms of the proposed D FlipFlops (a)Design-I (b) Design-II.

3. CONCLUSIONS

This paper proposes a new flip-flop design that integrates GALEOR and ONOFIC techniques to improve power performance. By introducing only two gated leakage transistors in design-I and ON OFIC logic in design-II, the average power consumed by the circuit got reduced by 35.61% and 34.36% as compared to the previous design. These designs can be used in constructing register files, shift registers, counters, frequency dividers and other flip flop. The outcomes indicate that the proposed flipflop designs can be used in nano scale.

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