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6T and 8T SRAM Cell Simulation with Power Loss Analysis

A. Manikandan*

**Assistant Professor, ECE Department, SSM Institute of Engineering and Technology, Dindigul, India*

*Corresponding Email: *manikandan.aapece@ssmiet.ac.in*

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Abstract: Reducing the power consumption in a VLSI circuits is a prime concern now a days. Memory circuits play an important role in the design of electronic small power devices. Almost every digital systems is having memory as an important part in their design. The high speed circuits dissipate a considerable amount of power in a short time. In this paper conventional SRAM cell is modified little bit to reduce the dynamic power dissipation. The overall capacitance reduced by adding few extra transistors. Because of the fact that charging and the discharging of the bit lines consumes the most power , so 6T cell and 8T cell can be used to reduce the power by adding an extra number of transistors to the pull down path. In this paper 6T SRAM cell as well as 8T SRAM cell simulated and their performance compared in terms of power dissipation.

Keywords: Power Dissipation, SRAM Cell, Power Dissipation, Tanner Tools, VLSI.

1. INTRODUCTION

Low power consumption and high performance are today's challenges. There is an increasing need to design portable devices that operate on low-power batteries and consume very little power. SRAM is an inherent part of most systems in the VLSI domain [1-5]. Speed and power consumption are key issues in designing SRAM circuits [6-8]. A traditional SRAM cell uses six transistors for reading and writing. It has the advantage of small footprint [9-12]. Here, reading and writing are done through a single bit line [13-15]. The logic is stable after writing, but reading requires additional circuitry such as sense amplifiers [16-20]. The conventional 8T circuit proposed in [21-24] is also simulated with conventional 6T batteries, and the transient analysis of the circuit is carried out, and the power consumption is calculated. Traditional circuits use eight transistors. The key idea of the 8T transistor used here is that the value stored in the SRAM cell is transferred through another transistor to get the read output [25]. This white paper focuses on the design and simulation of a traditional

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6T SRAM cell and an advanced 8T SRAM cell, and compares the power dissipation of the two cells. Simulations and analyzes done using generic 250nm model files. Result of We compared the power loss of a conventional 6T SRAM cell and an 8T SRAM cells [26-28].

RAM DESIGN

Conventional 6T SRAM cell

Figure 1 shows that a 6T SRAM cell [9] consists of PMOS and NMOS transistors. PMOS transistors are the load transistors and the lower NMOS transistors, which are connected in a cross-coupled way termed as the driver transistor. The pass transistor used to connect the cross-coupled inverter to the outside world. Word lines are used to activate or deactivate the memory writing, Data bits that have to be written are supplied via the bit lines.

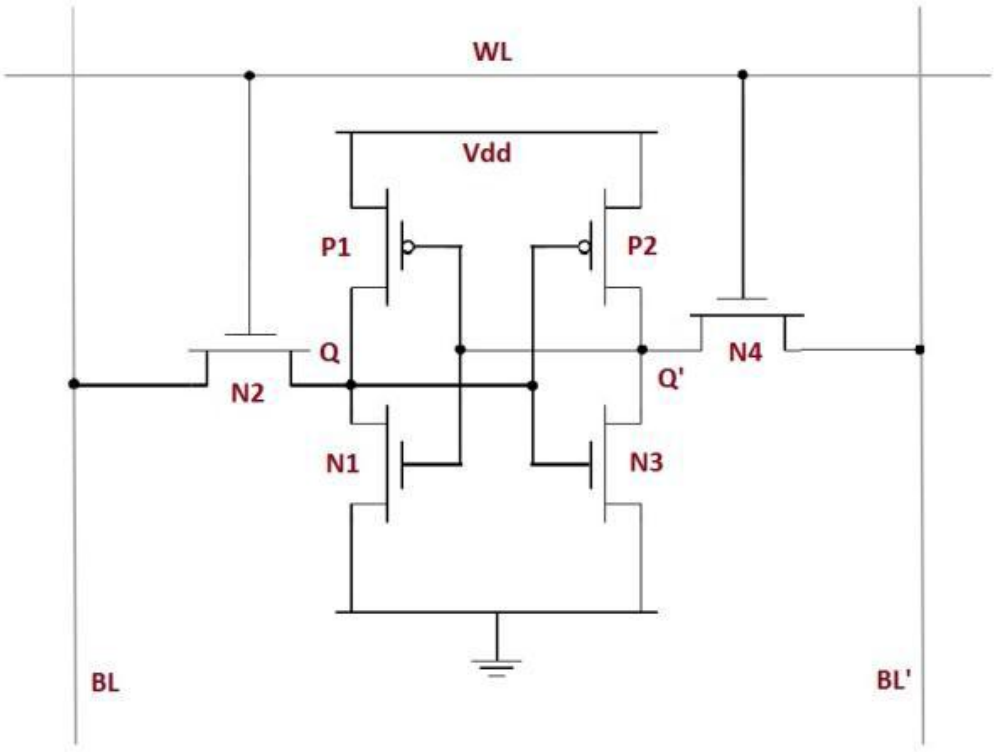

Fig 1. 6T SRAM cell

Bit lines are also used to read data stored in SRAM cells. In write mode, the bit to be written is provided on the bit line with the word line asserted, and the inverted version is provided on the bit bar line. When the word line is asserted, the bit line value is latched. As a bit line, the input drives much stronger than the value previously stored in the two cross-coupled inverters, so new data is written to the cell. To read a bit, the bit line is pre charged to a logic 1, then the word line is asserted, which activates the access transistor in the design. The value stored in the SRAM is transferred to the bit lines, one of which is discharged through the drive transistor and the other is pulled up to logic 1 via the load transistors.

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8T SRAM Cell

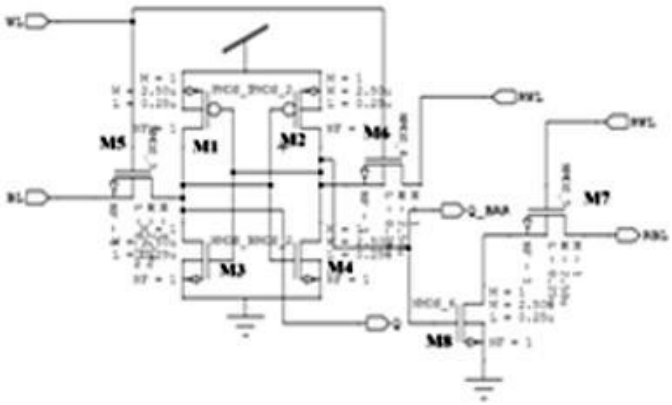

Fig 2. 8T SRAM Cell

8T SRAM cells [10] use separate sections for writing and reading stored bits. M5 and M6 are access transistors used to access the inverter during write operations. Transistors M1, M3, M2, and M4 are used to store data. M1 and M3 are one inverter (inverter 1), and M2 and M4 are another inverter. (Inverter 2) Two inverters are connected back to back. The access transistor is enabled or disabled depending on the value of WL. Six transistors are used to write data into the SRAM cell, and two transistors are used to read stored data. The read array is a separate section that is active during the read operation. When data needs to be written, the access transistor is activated. The data bits are provided via the bit lines (BL). In the write operation, the data comes via the M5 transistor and passes through the second inverter and the input of inverter 1 receives the inverted value from inverter 2 and value get stored at the node Q. This way, the write operation performed. For the read operation, the data stored will be transferred to RBL line when the RWL line is active.

Simulation

6T SRAM Write operation

For simulating the write operation of 6T SRAM cell, the cell designed using the schematic editor tool and then WL and BL lines are assigned proper signal and simulation performed for 2000ns.

8T SRAM write and read Operation.

For the 8T SRAM cell, the cell designed with the schematic editor and then proper bit streams are supplied in proper order to have a situation where some data are written first in the SRAM cell, then they are read via the RBL lines by activating the RWL line at the proper time. The simulation performed for 2000ns,

2. RESULTS AND DISCUSSION

Simulation Waveforms

In this section, we simulate the read and write operations of 6T and 8T SRAM cells by

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providing appropriate BL and WL signals at appropriate times. The 250 nm general library is used for this simulation. We also use the Tanner tool for design verification. In addition, we simulated the power loss of 6T and 8TSRAM cells in the case of bit "0" write and bit "1" write, and compared the power loss between 8TSRAM cells.

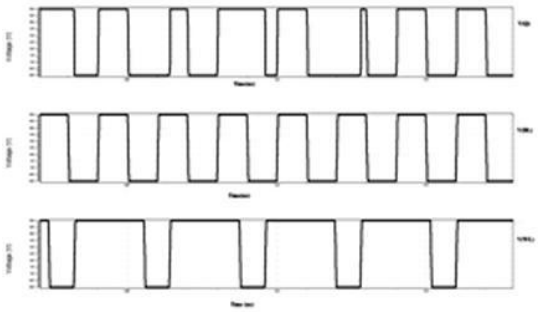

Fig 3. 6T SRAM write operation

In the Fig 3.shows the various signals during the SRAM write cycle. First logic 1 written to memory and after that logic 0 written. The data that is written also displayed in the waveform(Q).During the write operation the Word Line WL) lines must go to logic 1 state and either logic 0 or logic 1 can be written based on the logic provided via the Bit lines(BL).Then in Fig 4. various write cycle signals as well as the read cycle signals are shown for the 8T SRAM cell. The waveform shows how few data bits can be written into the cell and how the read operations can be performed by asserting the word line(WL) and the read word line(RWL) at proper time..All the simulations were performed for 2000ns.As seen from the waveform the read operation retrieves the stored data only when RWL is asserted.

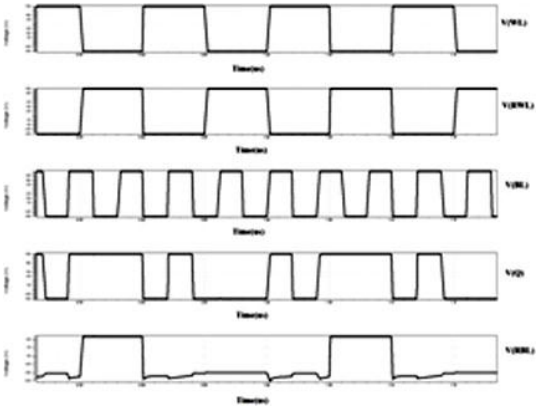

Fig 4. 8T SRAM write and read operation

Power dissipation

Table 1 shows the average power dissipated during the write 1 and write 0 cycle for 6T and 8T SRAM cell respectively. The table also shows the considerable amount of power saving when 8T SRAM simulated. This power dissipation table is for 250nm model and simulated with T-SPICE.

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Table 1 Average power dissipation

Operation	Average Power (6T cell)	Average Power (8T cell)	Save (%)
Write bit 1	2.3mW	2.1mW	8.69
Write bit 0	1.6mW	1.26mW	21

It has been observed from the table that '1' write cycle power dissipation reduced by 8.69% when 8T SRAM cell being used and the write 0 cycle power dissipation decreased 21 % .The above result found for 5V supply and 250nmtechnology.

Table 2 Variation of power dissipation with supply voltage for 8T SRAM

Operation	5V	1.8 V	1.2 V
Write bit 1	2.1mW	79uW	9.2u W
Write bit 0	1.26mW	53uW	9.03u W

Table 2 shows the power dissipation for different supply voltages for 8T SRAM cell and found ideal for low voltge devices for which case the power dissipation Is very low.

3. CONCLUSIONS

As seen from this paper, the average power reduced to 21% in the case of 0-bit writing and 8.69% in the case of 1-bit writing. From this, it can be concluded that the 8T SRAM device will consume very little power as compared with the conventional 6T SRAM cell, whose results are also reported in this paper.

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