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Switching Sequence Control 31-Level Asymmetric Cascaded of Reduced Switch Count Multilevel Inverter with Multi Carrier Pulse Width Modulation

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Abstract: ***Various pulse width modulation techniques, including as cascaded multilevel inverters (MLI), diode clamped multilevel inverters, and flying capacitor multilevel inverters, can be used to simply operate common inverters. Due to increased switching losses, current MLIs cannot reach high efficiency. Due to lower losses and THD than standard MLI topologies, the asymmetric cascaded multi-level H-bridge inverter architecture examined in this white paper employs fewer switches and more output voltage levels (Total Harmonic Distortion). The THD is less than the IEEE standard because of the suggested architecture. In this instance, phase difference (PD) multi-carrier PWM techniques are used to control the gate pulses using sinusoidal reference. Each switch receives a different pulse pattern thanks to a method of decimal-to-binary conversion. It is possible to utilise the suggested circuit for applications requiring moderate to high power, and it is quite simple to evaluate. Utilize the MATLAB/SIMULINK environment to simulate time-domain behaviour for the 31-level and 33-level multilevel inverter topologies.***

Keywords: ***Multilevel Inverter, PDPWM, Pulse Pattern, Reduced Switches, Multi Carrier Unipolar Pulse Width Modulation, Reduced Switch Multilevel Inverter, Switching Sequence, Total Harmonic Distortion.***

1. INTRODUCTION

Recent advancements in the field of power sensors have made use of multilayer inverters for medium to high power applications, primarily integrating renewable energy with FACTS devices [1]. It almost seems like a sine wave when looking at the output voltage waveform. The ability of multilayer inverters to meet additional power ratings and power quality standards related to

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lowering harmonic distortion and electromagnetic interference makes them desirable in power electronics applications. High switching frequency and fundamental switching frequencies are both operable for multilevel inverters [2]. Three topologies for multilevel inverters that are frequently utilised are flying capacitor (FC), cascaded H-bridge (CHB), and neutral clamp (NPC) [3]. Because each module still requires its own DC power supply, despite the cascaded H-bridge topology being simpler and more modular than other topologies like NPC and FC, it is frequently employed in this field and has garnered a lot of interest.

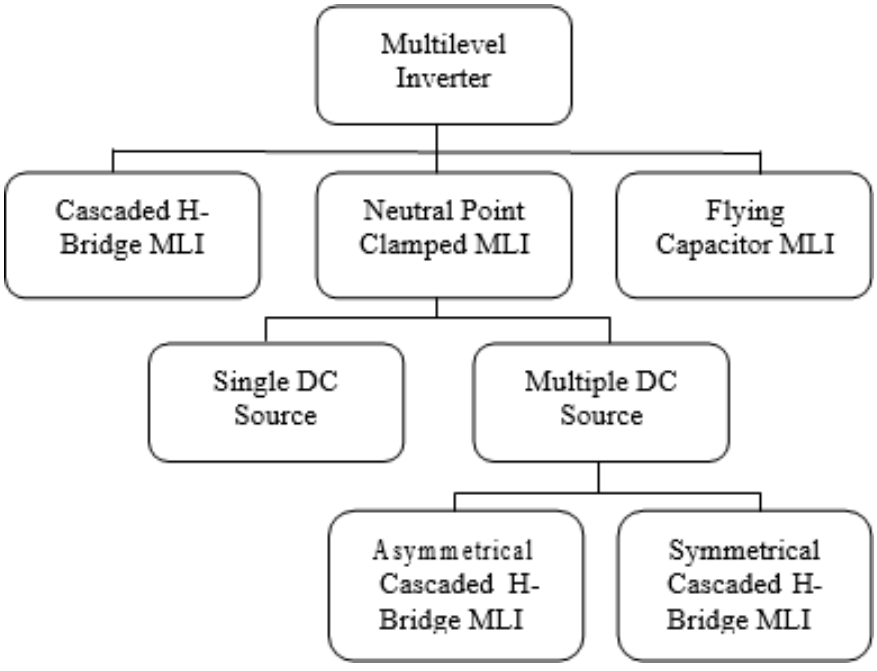

Figure 1: Flow Chart of MLI Topologies

Two different types of CHB topologies—symmetric CHB and asymmetric CHB—can be distinguished based on the magnitude of the DC voltage. Asymmetric topologies use fewer switches, DC power supply, and diodes at the same voltage level as symmetric topologies [1]. As it uses fewer switching elements and produces less overall harmonic distortion than the standard architecture, the suggested MLI topology offers various benefits.

Literature Survey

[4] It is advised to utilise the least number of capacitors and switches necessary to disable the sub-multilevel converter switches' series minimum standby voltage in order to achieve the highest output voltage level. A novel approach can estimate the size of the DC voltage source. A 53-level converter running in single-phase with a minimal number of switches is supported by experimental data that demonstrates its functionality and effectiveness.

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A few switches are used in the inverters that may switch DC supply voltages in series and parallel shown in [5]. The 11-level inverter's performance and functionality will be experimentally verified based on the suggested topology. The lower multi-level inverter basic device, instance [6], is a prime example of a basic device that can be coupled in series to produce a cascaded multi-level inverter. The operation of an experimentally verified 300V 11-level shifter at the output is confirmed using three distinct techniques for scaling the DC voltage source.

Using an 11-level symmetric inverter with fewer switches and a 15-level asymmetric inverter with 15 levels, [7] experimentally validate the behaviour of the suggested topology. A series connection can be made between several sub-multilevel inverters, as shown in [8]. The new topology will test 13-level symmetric and 31-level asymmetric inverters in order to decrease switching quantity, DC voltage source, and switching constant voltage.

A cascaded multilayer inverter with few switching elements is depicted in [9] as having a simple layout. The three cascaded H-bridge topology is thought to be the best topology for asymmetric circumstances, according to the authors. For both symmetric and asymmetric scenarios, you can extend the provided topology. Both 13-level and 25-level asymmetric inverters will be subjected to experimental verification. The generation of asymmetric MLIs made up of DC voltage sources of different sizes is suggested by [10] using a series of connected SI-based devices. We suggest an algorithm that can figure out how big a DC voltage source should be in order to reduce the amount of power switches. An experimentally verified 17-level asymmetric inverter is used to implement the suggested design.

The [11] figure depicts a multilayer inverter with a changeable input DC power source connected with power switches in the opposite direction. The input DC level is shown as a staircase waveform whether it is mixed with other input levels or shown alone. Assume that the input comes from the same DC sources across the board.

Unidirectional switches and H-bridges are used to create all voltage levels in the innovative cascading multilevel inverter scheme presented in [12]. Using two distinct topologies and an algorithm for sizing a DC voltage source, a straightforward 7-level inverter is described. This fundamental unit can be expanded to produce many output levels. On a 31-level inverter with low power switches, experimental validation is carried out.

To decrease the number of power electronic devices, [13] proposed a technique based on the series connection of several switching capacitor base cells. A DC voltage source can be sized using either of two approaches. Experiments have shown that this architecture can generate 25-level and 17-level single-phase inverters. A 7-level symmetric switched diode converter and a 15-level asymmetric switched diode converter, both requiring fewer power electronics, were shown in [31] as experimental configurations.

Using patented H-bridge technology, [14] suggested a single-phase cascaded multilevel inverter. The DC voltage source can be sized to generate any output voltage level by choosing from nine different methods. Analysis of the algorithms' advantages and disadvantages is recommended.

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All suggested topologies aim to lower the DC voltage sources, switches, and power electronics' breaking voltages. The experimental verification is conducted using the 9th-order algorithm and the 49-level single-phase inverter's functionality.

Inverters with fewer switches can be cascaded together to create lower multi-layer inverters, according to [15]. To calculate the size of the DC voltage source, formulas are also given. 15-level sub-multi-level inverters and 25-level string inverters are used in the experiment to examine performance and operation.
[16] showed a simple system that produced a multilayer output using five switches and three voltage sources connected in series. A DC voltage source's size has been determined using four different ways. In order to reduce the amount of power electronics required by the suggested design, an experimental examination of a 15-level inverter is conducted. In [35], the modular design of symmetrical VSI is displayed. Power electronics and status switches are not frequently utilised together. Based on the suggested topology, a nine-level experimental inverter is confirmed.
Using a limited number of power switches, [17] shown how to connect several basic devices in series. For calculating a DC voltage source's magnitude, two distinct techniques have been suggested. Utilizing the first approach, we acquire the DC voltage source for the suggested 21-level inverter and experimentally confirm its functionality.

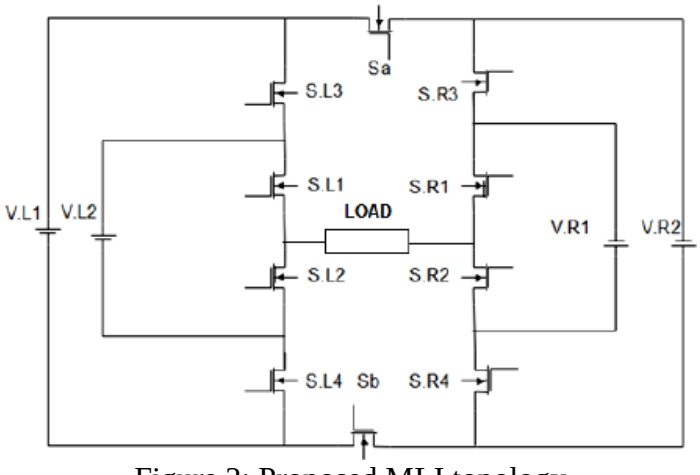

Figure 2: Proposed MLI topology

The highest output voltage for each cathode and anode of a 33-level inverter with four DC sources is 336V. Up to 315V and -315V negative output voltages are produced using a 31-level inverter using four DC sources. Four DC power supply are used in parallel by the H-bridge inverter. Switches S.L1, S.L2, S.L3, S.L4, S.R1, S.R2, S.R3, Sa, and Sb allow the four DC sources to be linked or unconnected to produce different voltages. The direction of current flow determines the load's output of AC, which is controlled by switches S.R1, S.R2, S.R3, and S.R4. A conventional

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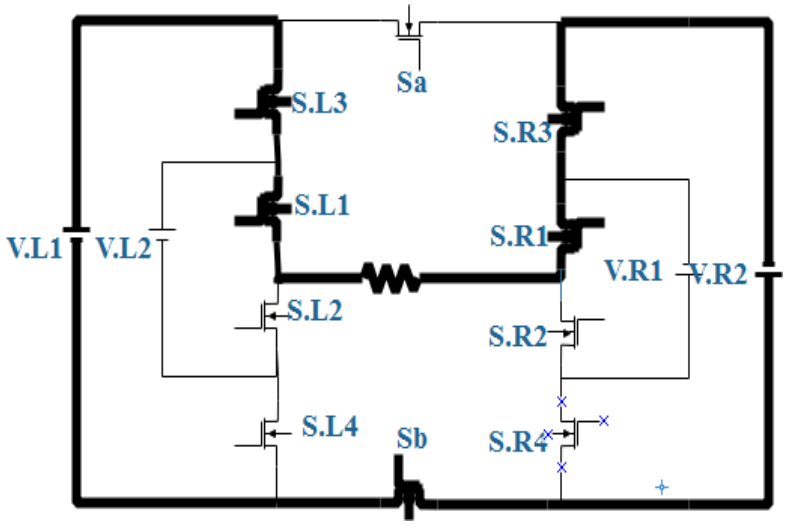
cascaded MLI needs n DC power supply, n switches, n levels of output, and n on-state switches. Using just 10 switches and 4 DC power supply, the suggested architecture can produce output voltages at levels 31 and 33.

33 inverters are suggested, i.e., connect the voltage level, taking into account the maximum DC containing Vdc/33, 2Vdc/33, 3Vdc/33, 4Vdc/33, 5Vdc/33, 6Vdc/33, 7Vdc/33, 8Vdc/etc. As of this writing, the following output voltage ratings are listed: 9Vdc/33, 10Vdc/33, 11Vdc/33, 12Vdc/33, 13Vdc/33, 15Vdc/33, 16Vdc/323, 3/17, and 29Vdc/33 in Figure 2 [11]. The voltage level for mode m, taking the variable m into account, is (m-1) / 33. In the negative position, the same voltage level is generated. The 33-level H-bridge architecture has various benefits over other topologies, including fewer power switches and decreased THD. S. Excluding L1, L2, L3, L4, S.I.I. R1, R2, and S. Switch states "off" and "on" are indicated by the indicators "0" and "1," respectively. According to this switching situation, the IGBT switch functions and produces a multilayer waveform. H-bridge IGBT switching pulses are controlled using the Sincos PWM approach (SPWM). In this instance, when the IGBT pairs appear simultaneously, positive and negative cycle waveforms are produced. Assume switches S.L3, S.L1, S.R2, and S.R4 are also "on," just as switches S.R3, S.R1, S.L2, and S.R4 are. occur. It may or may not be "closed" depending on how benign it is. A negative point will also be reached. The switches S.R3, S.L3, S.L1, S.R2, and S.R4 are "off" when S.R3, S.L1, S.R2, and S.R4 are "on."



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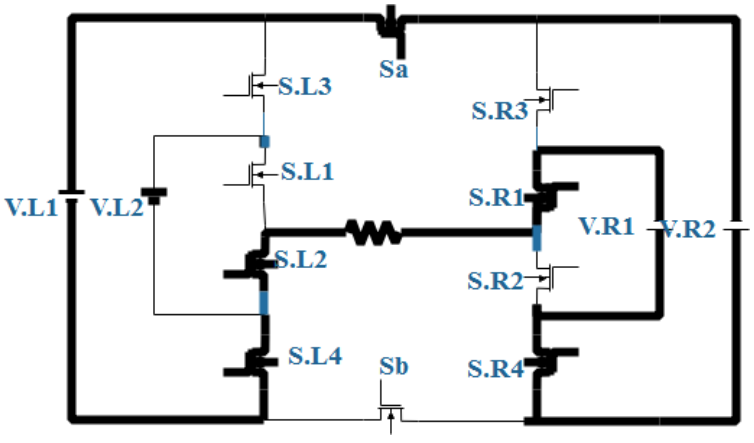

Figure 3: Mode 1 and Mode31 of operation of the proposed MLI topology for producing the DC link Voltage

Modulation Technique

While PWM (Pulse Width Modulation) uses the inverter's fixed DC input voltage to control the creation of the AC output voltage, it also uses the same constant DC input value to regulate the output voltage inside the inverter itself.

Phase Disposition Pulse Width Modulation

The only carriers used in this level-shifted multi-carrier pulse width modulation technique are carriers with the same phase. The reference signal is a sine wave with a frequency of 50 Hz, and the test signal is a triangular carrier with a frequency of 2 Khz. For the MOSFET, the output serves as the gate signal.

2. SIMULATION RESULTS

The suggested MLI architecture in Figure 4 is simulated by the Matlab/Simulink system. A simulation circuit is made up of two IGBTs and eight IGBTs (S.L1, S.L2, S.L3, S.L4, S.R1, S.R2, S other branches) on R3 and S.R4. The circuit's upper and lower arms are where (Sa and Sb) are situated. There are four DC voltage sources in all in the circuit. The rated voltages of V.L1 and V.L2 are, respectively, 42V, 210V, 42V, 105V, and 21V. Additionally, 5kHz is the setting for both the switching frequency (fs) and load resistance (R). Vdc is assumed to be 21V in this scenario.

Switching pulses are converted into positive and negative cycles and sent to the H-bridge circuit using a standard sinusoidal pulse width modulation (SPWM) technique. This pulse intersection generates the carrier signal and the reference signal. To produce pulses, every switch is delayed. 50 Hz is the frequency of the reference sine wave, while 5 kHz is the frequency of the carrier wave. The 31-level inverter array's output voltage and current waveforms are displayed in Figures 5 and 6.

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The output voltage and current FFT spectra of the 31-level inverter are displayed in Figures 7 and 8, respectively. The THD produced in this situation is composed of a voltage of 1.48 percent and a current of 1.2 percent. As a result, the THD gradually drops as the layer count rises.

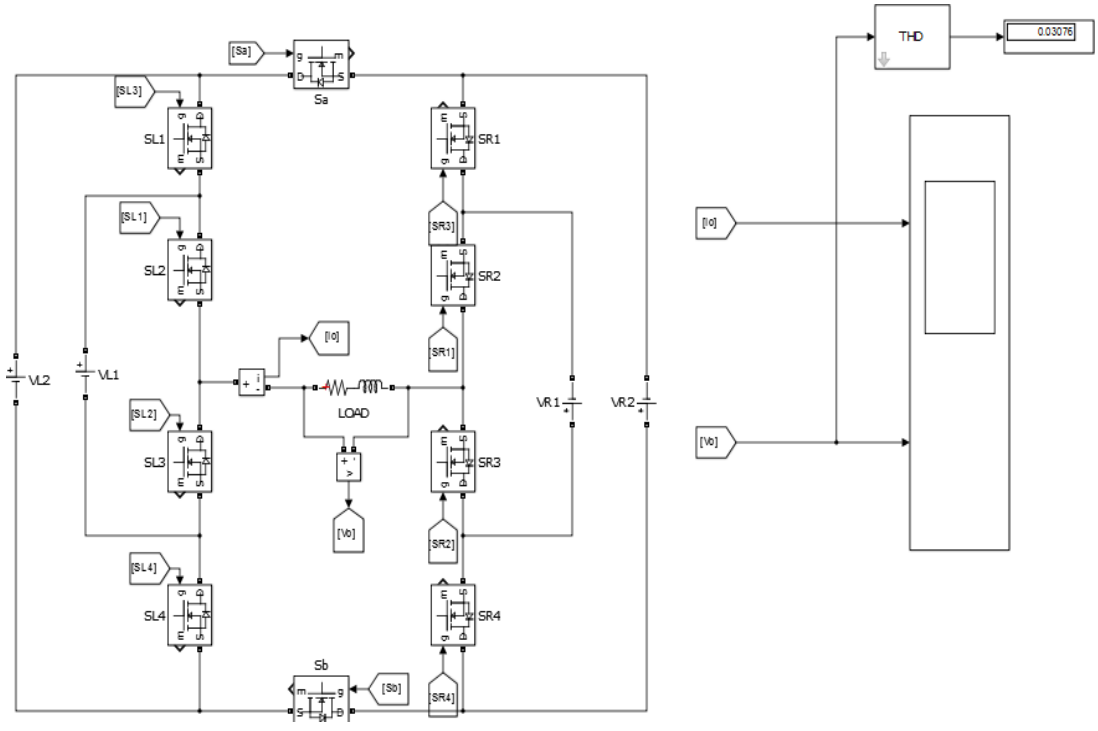

Figure 4: Simulink circuit of the proposed MLI topology

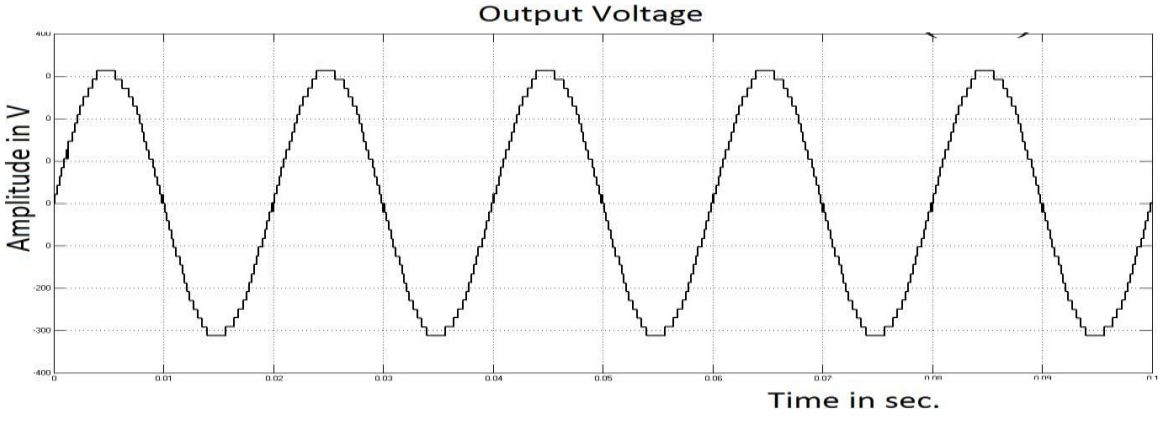

Figure 5: Output voltage waveform of 31-level inverter

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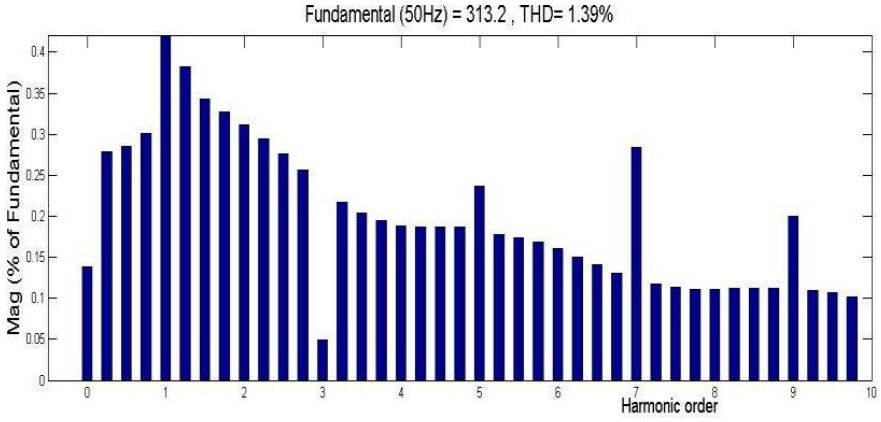

Figure 6: FFT plot for output voltage of 31-level inverter

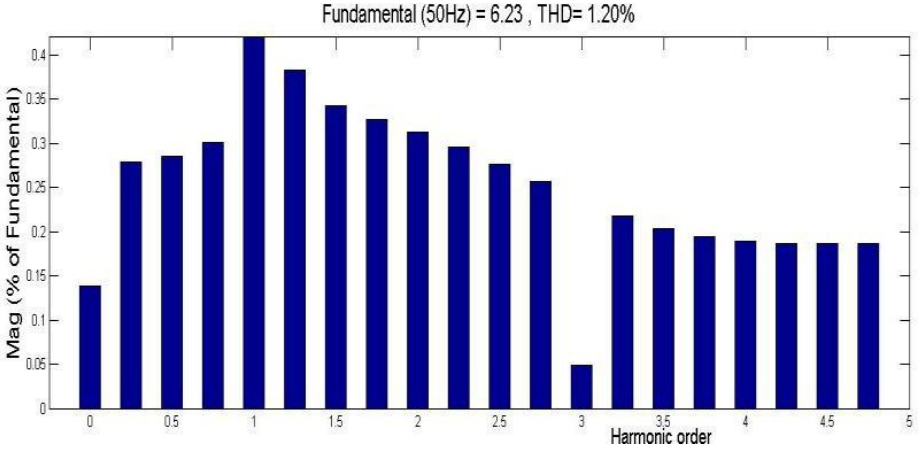

Figure 7: FFT plot for output current of 31-level inverter

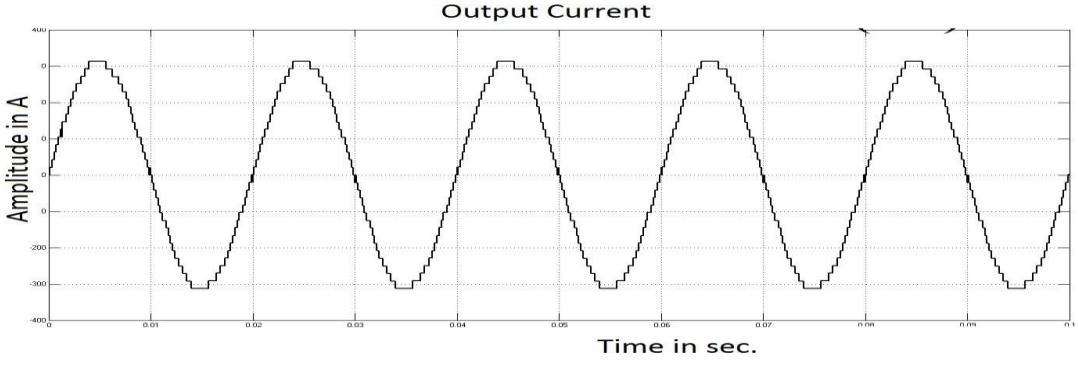

Figure 8: Output current waveform of 33-level inverter

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3. CONCLUSION

As part of this challenge, a 33-level cascaded multilevel inverter for single-phase circuits was assessed and simulated using the MATLAB/SIMULINK platform. The suggested way to run the inverter is multi-carrier pulse width modulation. The key outcome of this control strategy is to get rid of the output filter while bringing the THD (Total Harmonic Distortion) down to a level that is near to a sine wave. All suggested designs minimise the quantity of switches, drive circuits, and DC power sources.Reduced switching losses, fewer switches, and better output voltage capabilities are all benefits of using an inverter. The proposed architecture is evaluated against a 31-level inverter in terms of THD performance. A 33-level MLI produces an output voltage THD that is roughly 1.39 percent lower than a 31-level MLI with a THD of about 1.48 percent.

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